Fig.1

(PRIOR ART)

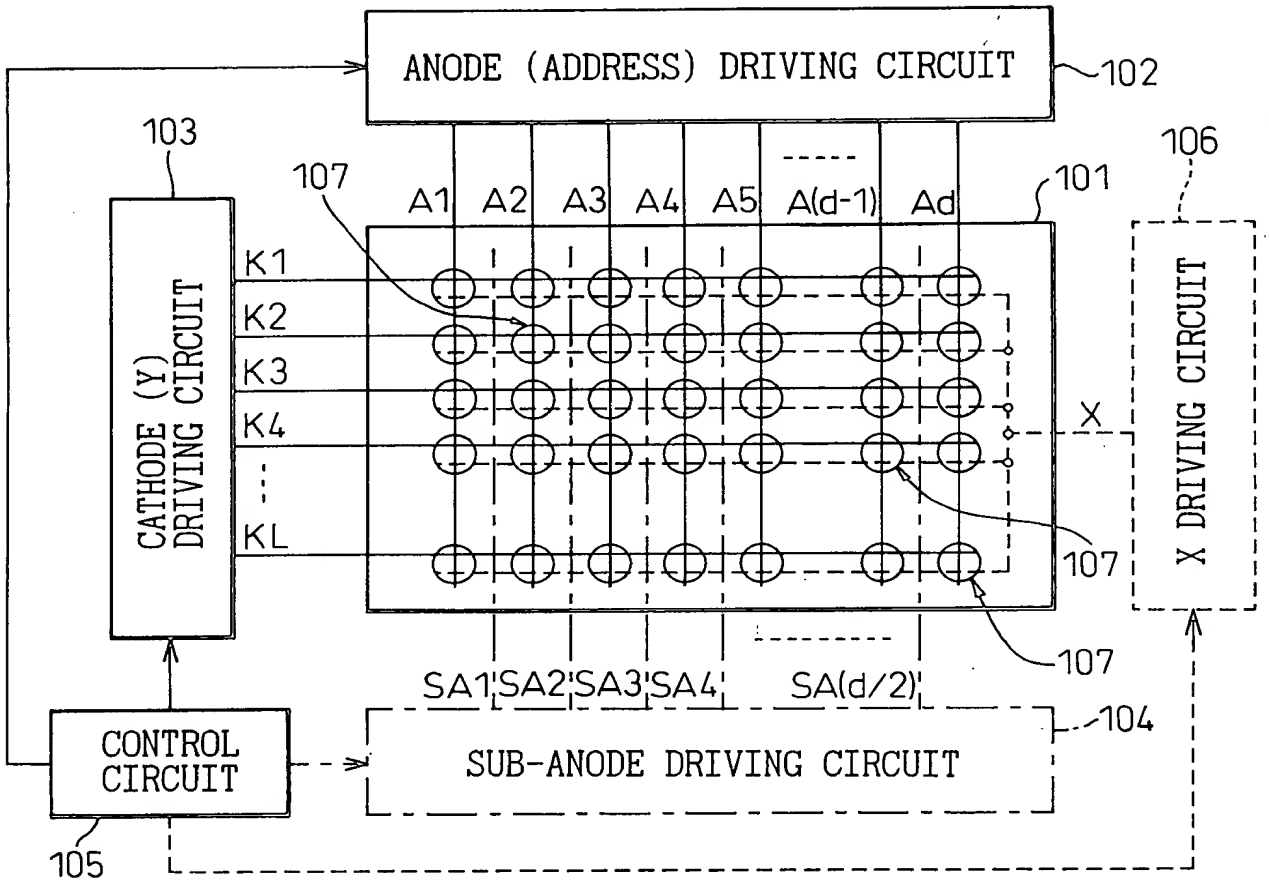


Fig.2

(PRIOR ART)

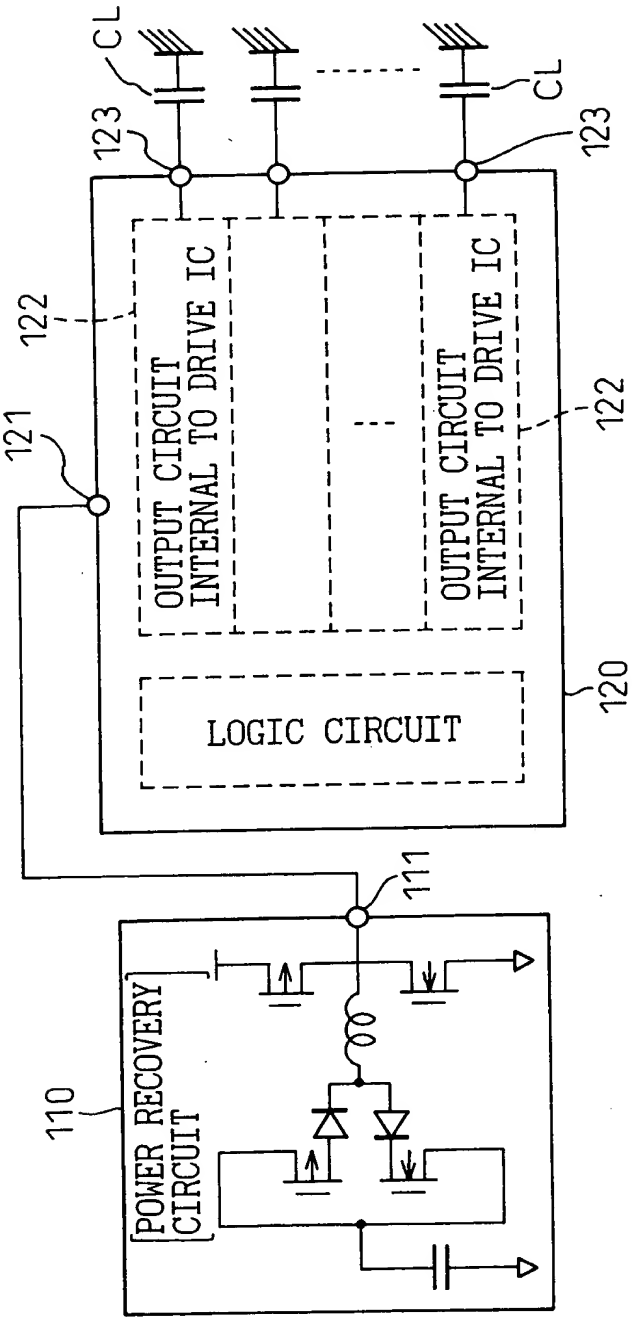


Fig.3

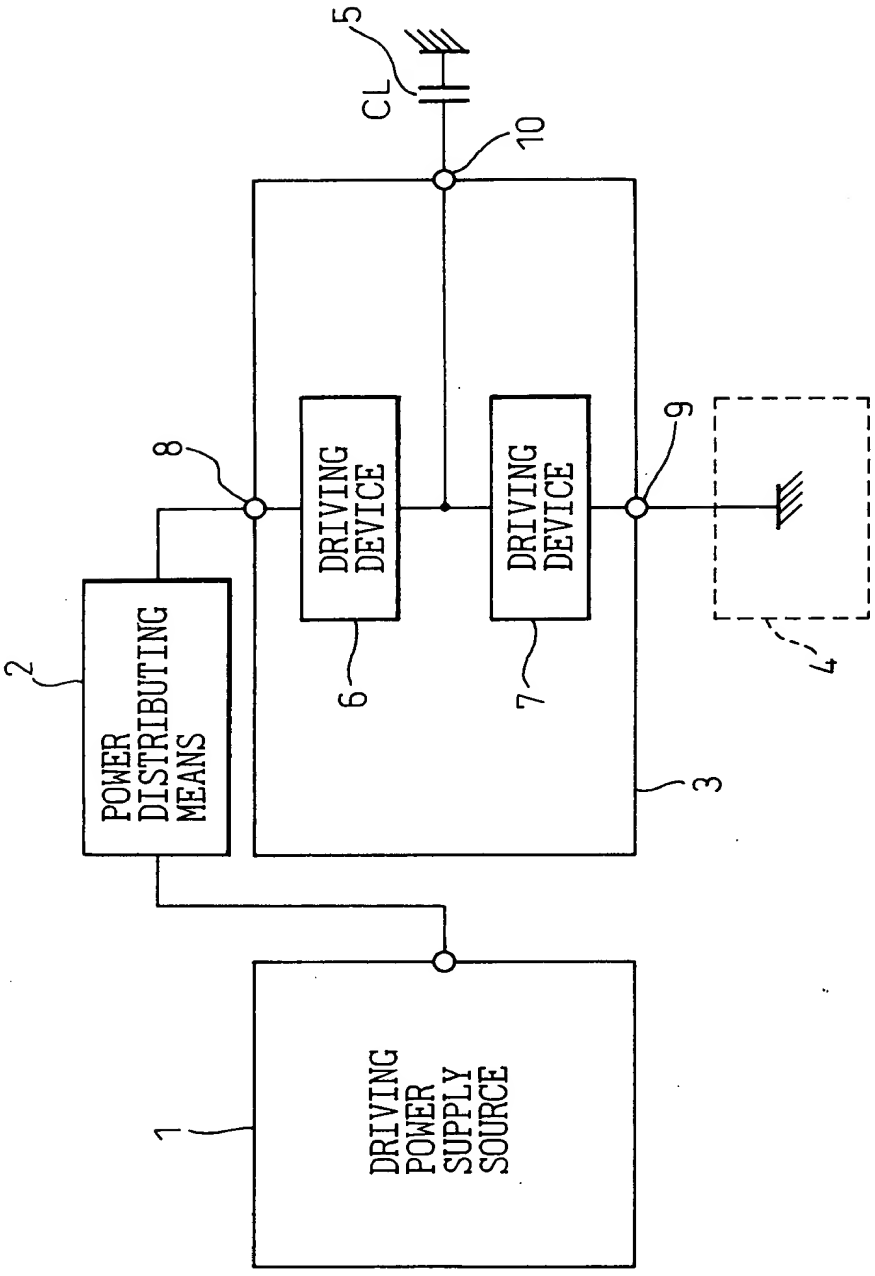

DRIVING POWER SUPPLY SOURCE
1
POWER DISTRIBUTING MEANS
2
3
DRIVING DEVICE
6
DRIVING DEVICE
7
8
9
10
CL
5
4

Fig.4

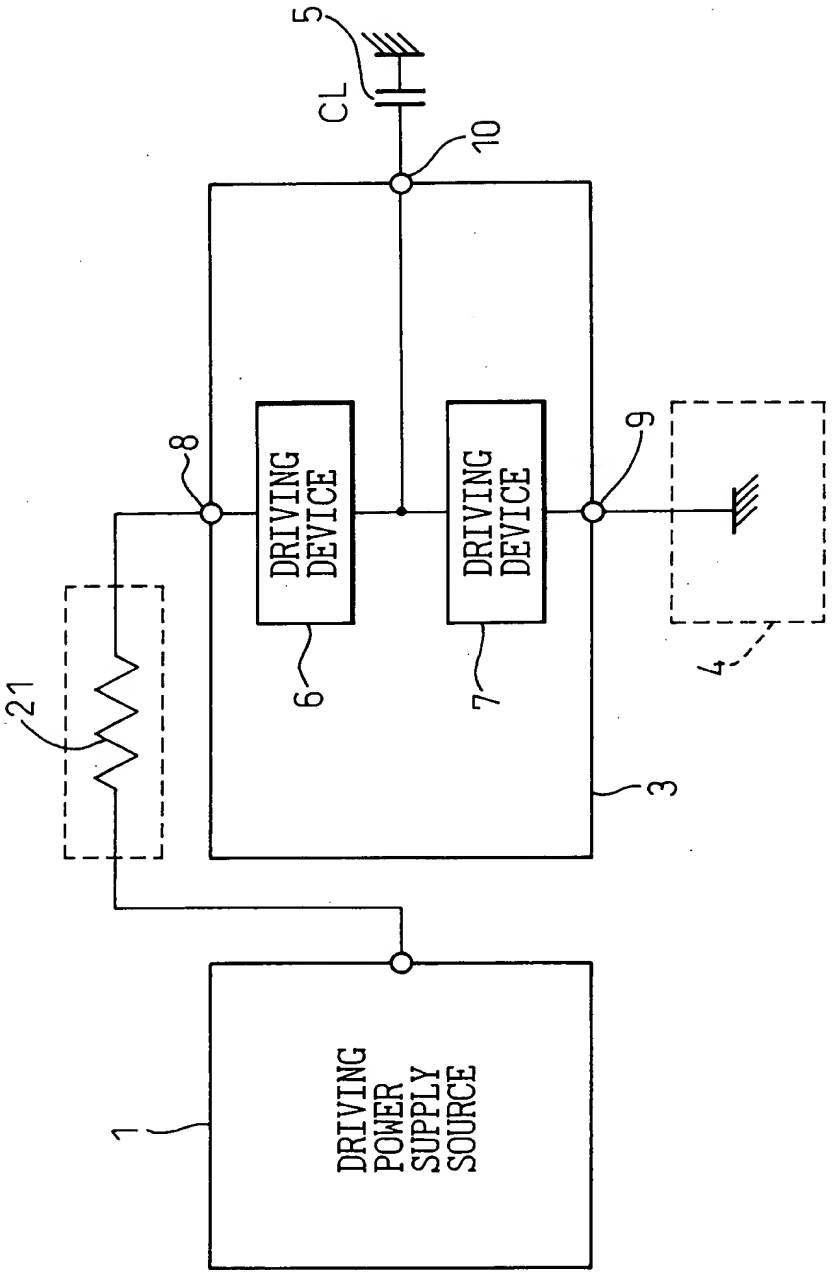

DRIVING POWER SUPPLY SOURCE
1
DRIVING DEVICE
DRIVING DEVICE
6
7
8
9
10
CL
5
21
3
4

Fig.5

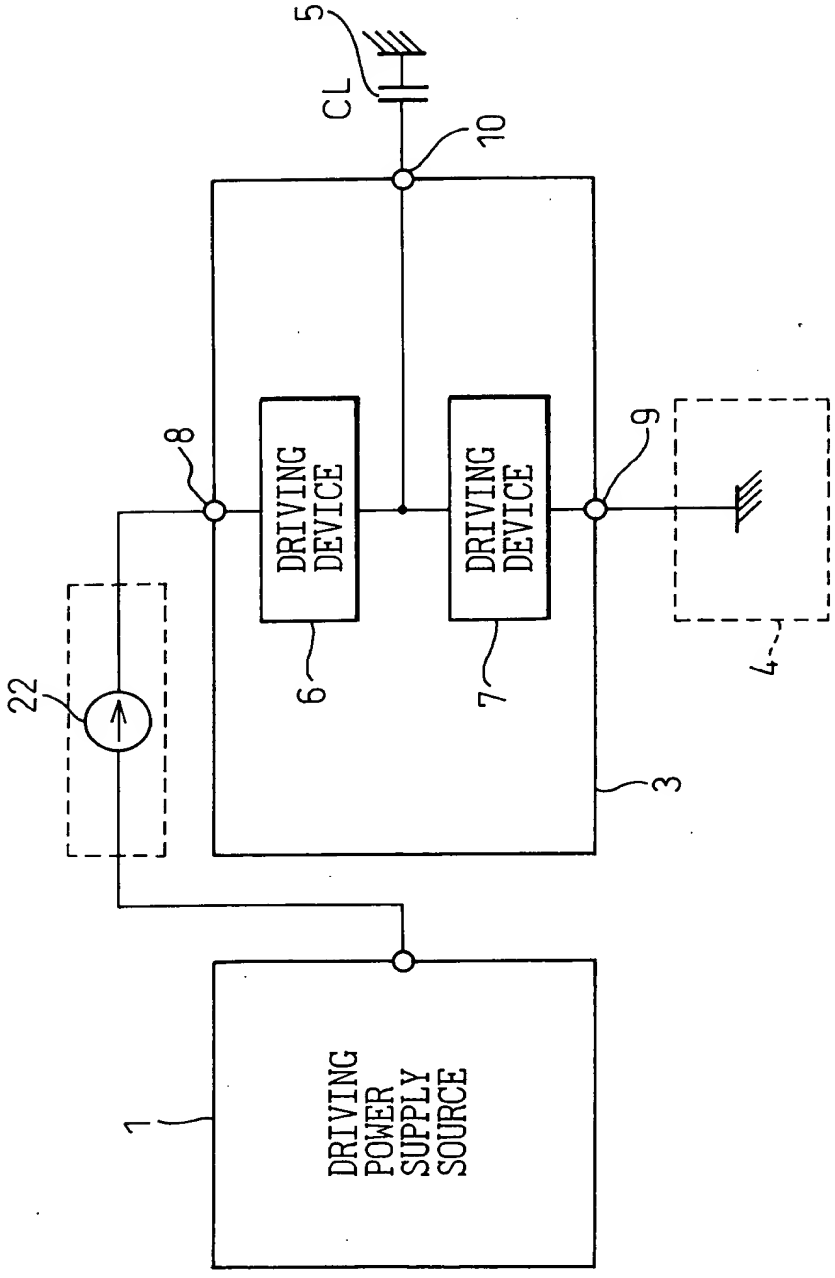

DRIVING POWER SUPPLY SOURCE
1
DRIVING DEVICE
6
DRIVING DEVICE
7
8
9
10
CL
5
22
3
4

Fig.6

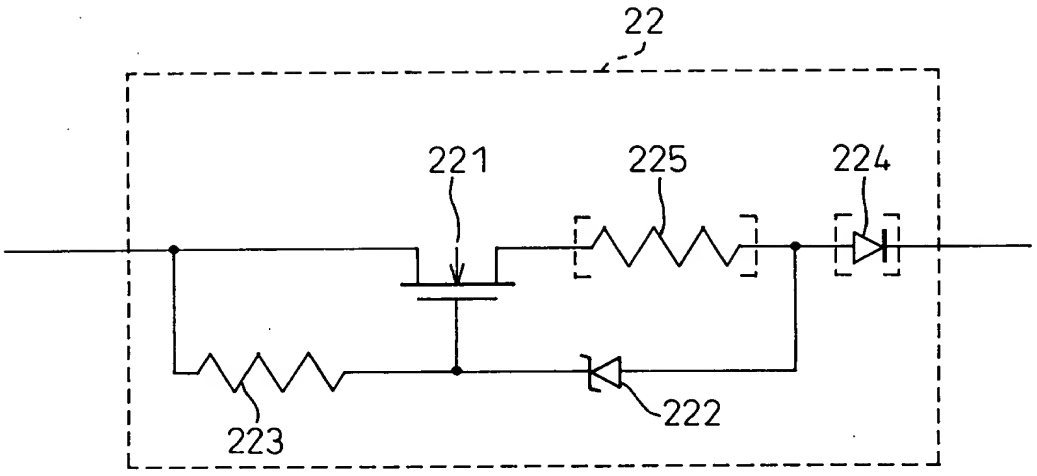


Fig.7

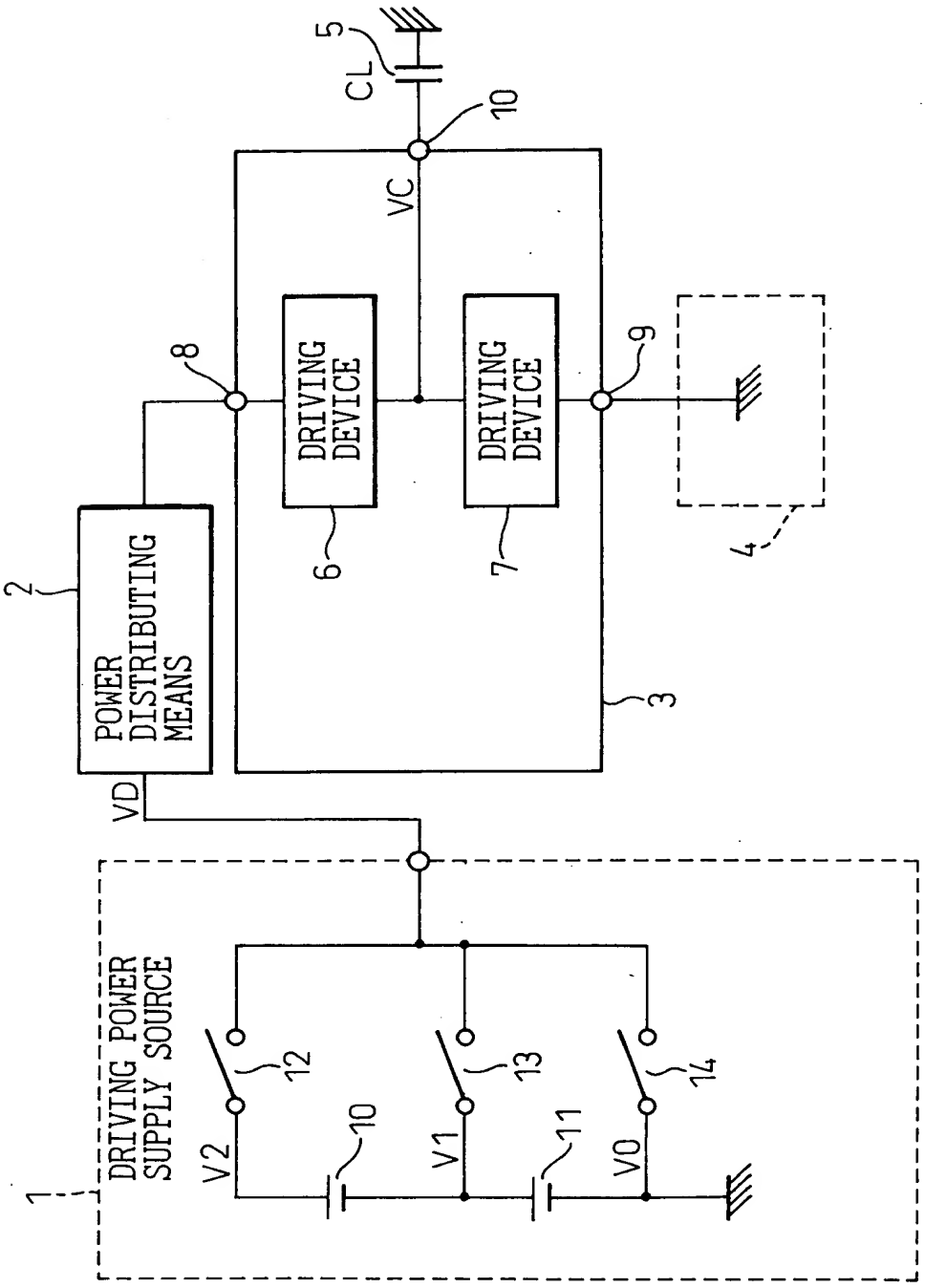

DRIVING POWER SUPPLY SOURCE
1
V2
V1
V0
10
11
12
13
14
VD
POWER DISTRIBUTING MEANS
2
3
DRIVING DEVICE
6
DRIVING DEVICE
7
8
9
4
VC
10
CL
5

Fig.8

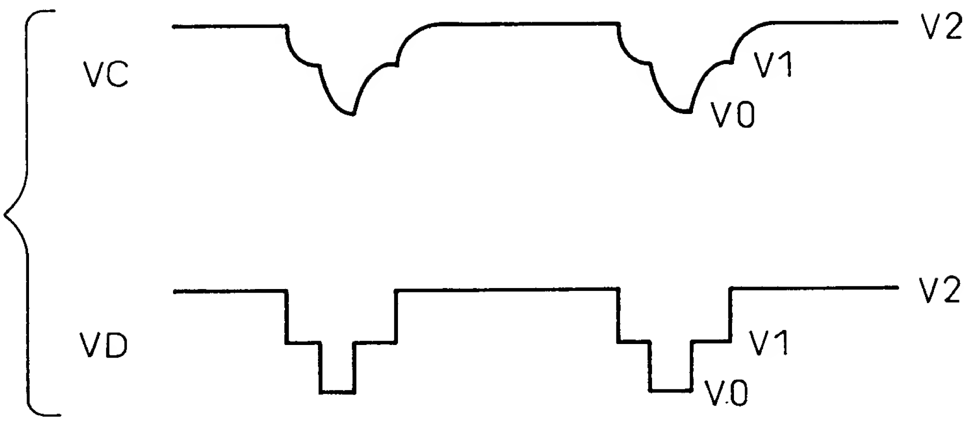


Fig.9

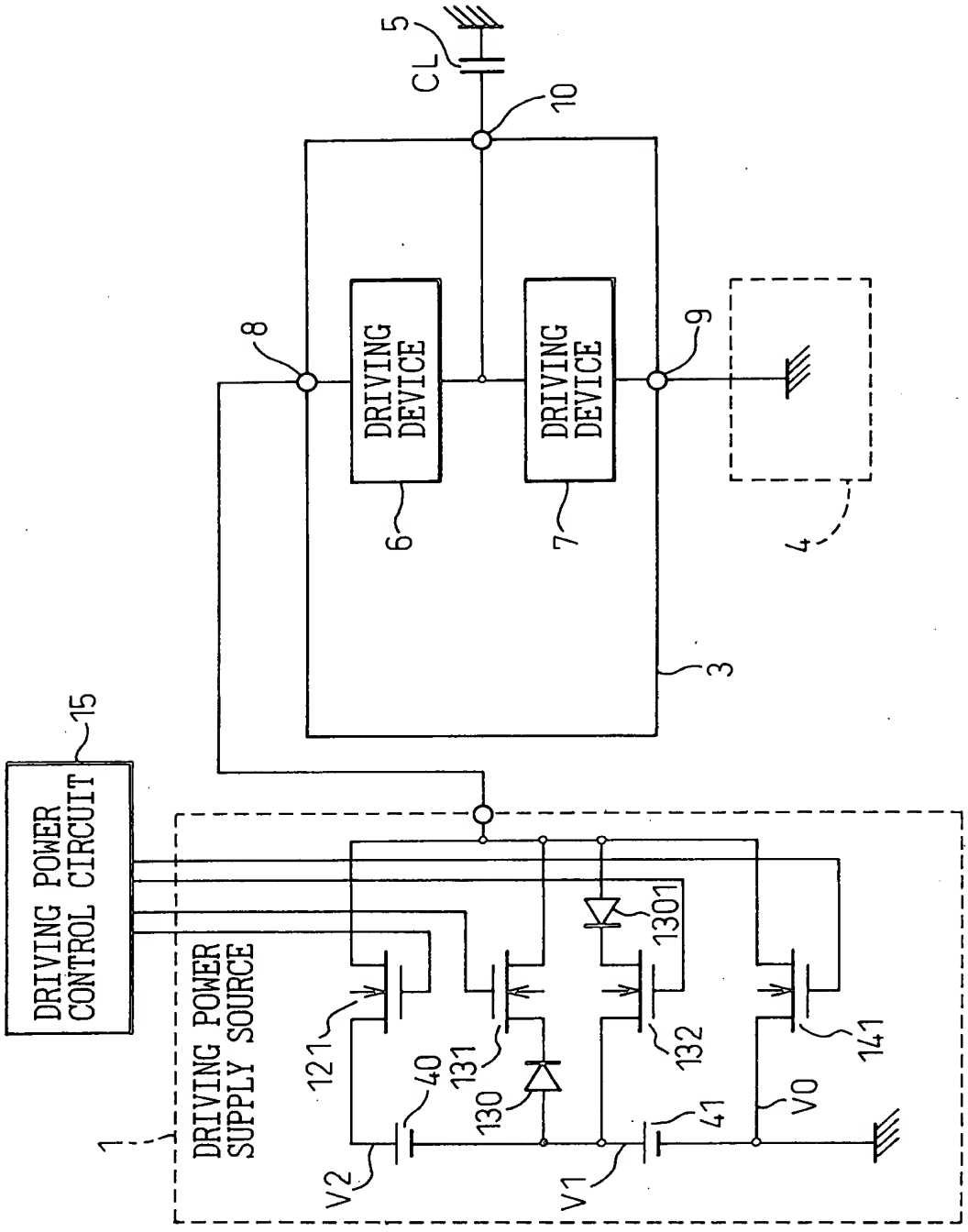

DRIVING POWER CONTROL CIRCUIT
15
DRIVING POWER SUPPLY SOURCE
1
DRIVING DEVICE
DRIVING DEVICE
6
7
8
9
10
CL
5
4
3
121
40
131
130
1301
132
41
141
V0
V1
V2

Fig.10

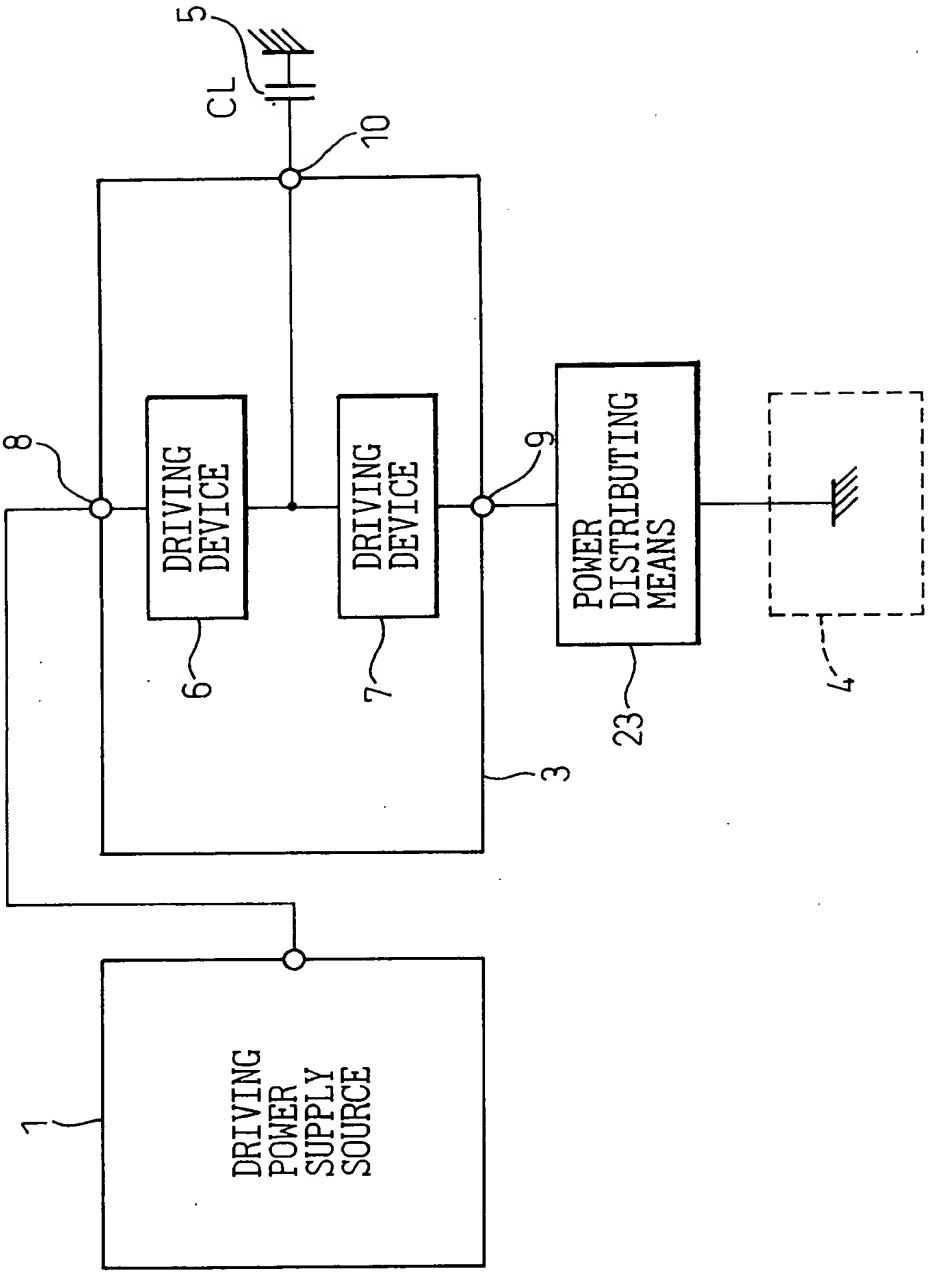

DRIVING POWER SUPPLY SOURCE
1
DRIVING DEVICE
6
DRIVING DEVICE
7
8
9
10
CL
5
3
POWER DISTRIBUTING MEANS
23
4

Fig.11

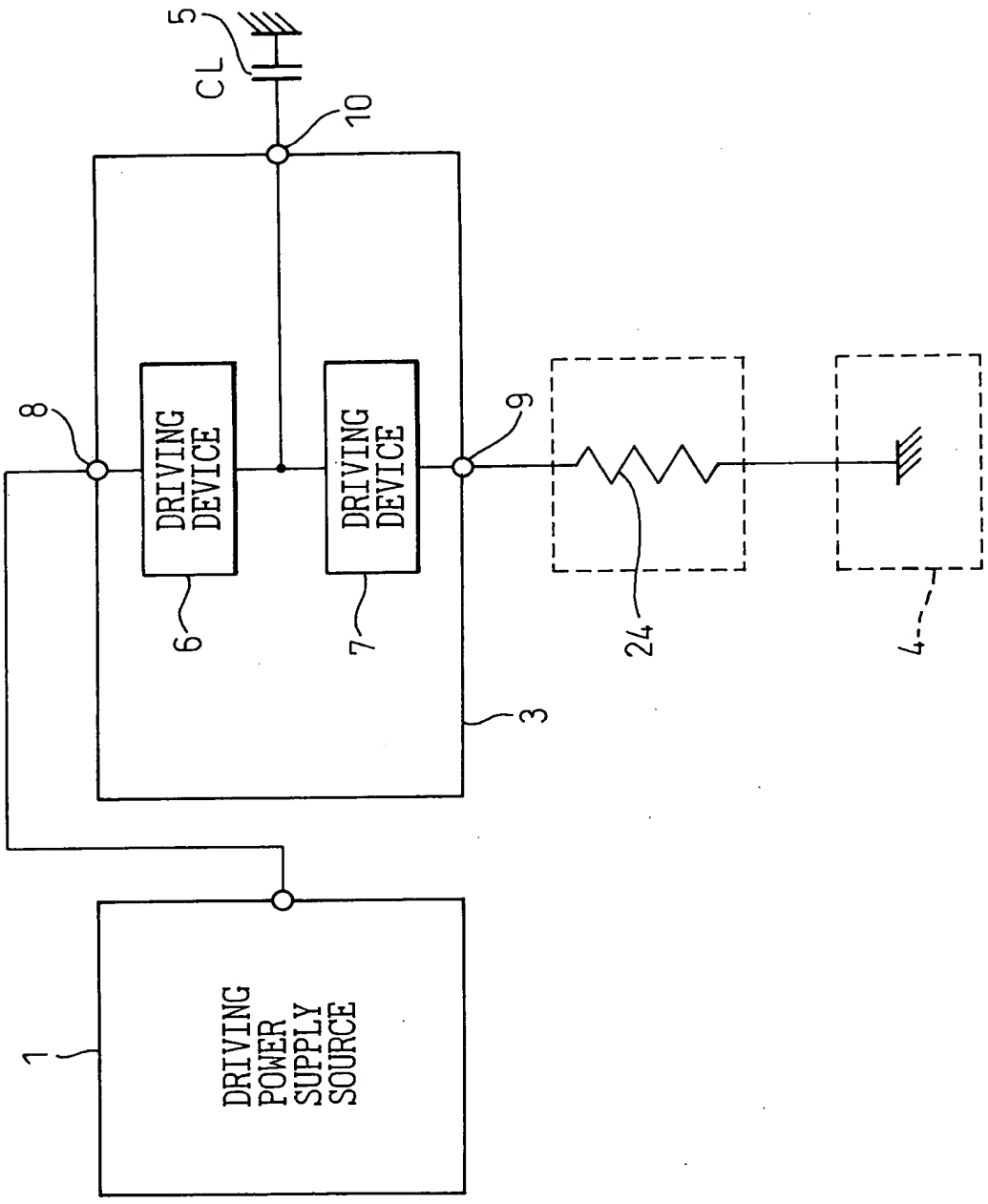

5
CL
10
8
DRIVING DEVICE
DRIVING DEVICE
9
6
7
24
4
3
1
DRIVING POWER SUPPLY SOURCE

Fig.12

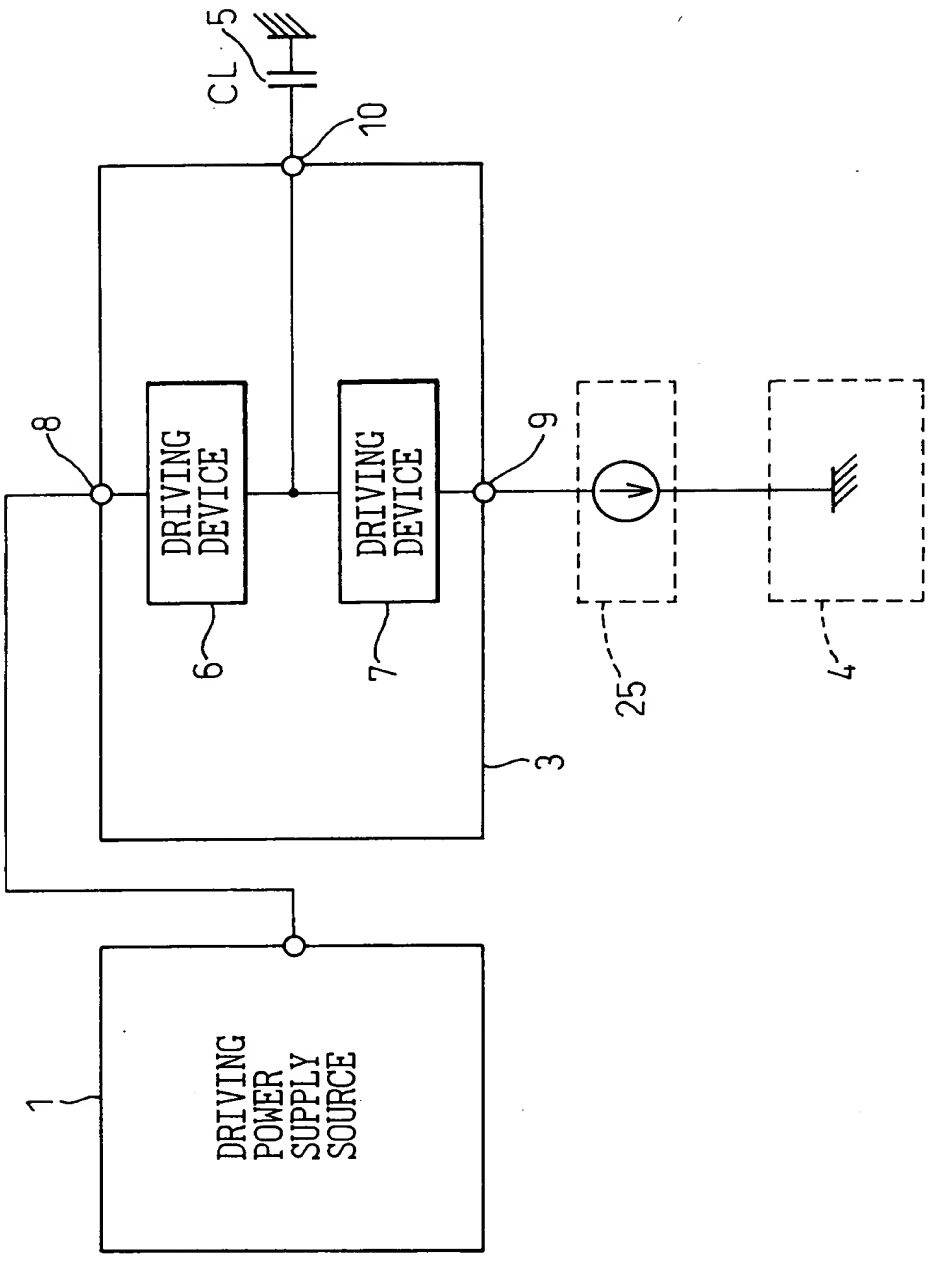

DRIVING POWER SUPPLY SOURCE
1
DRIVING DEVICE
6
DRIVING DEVICE
7
8
9
10
CL
5
3
25
4

Fig.13

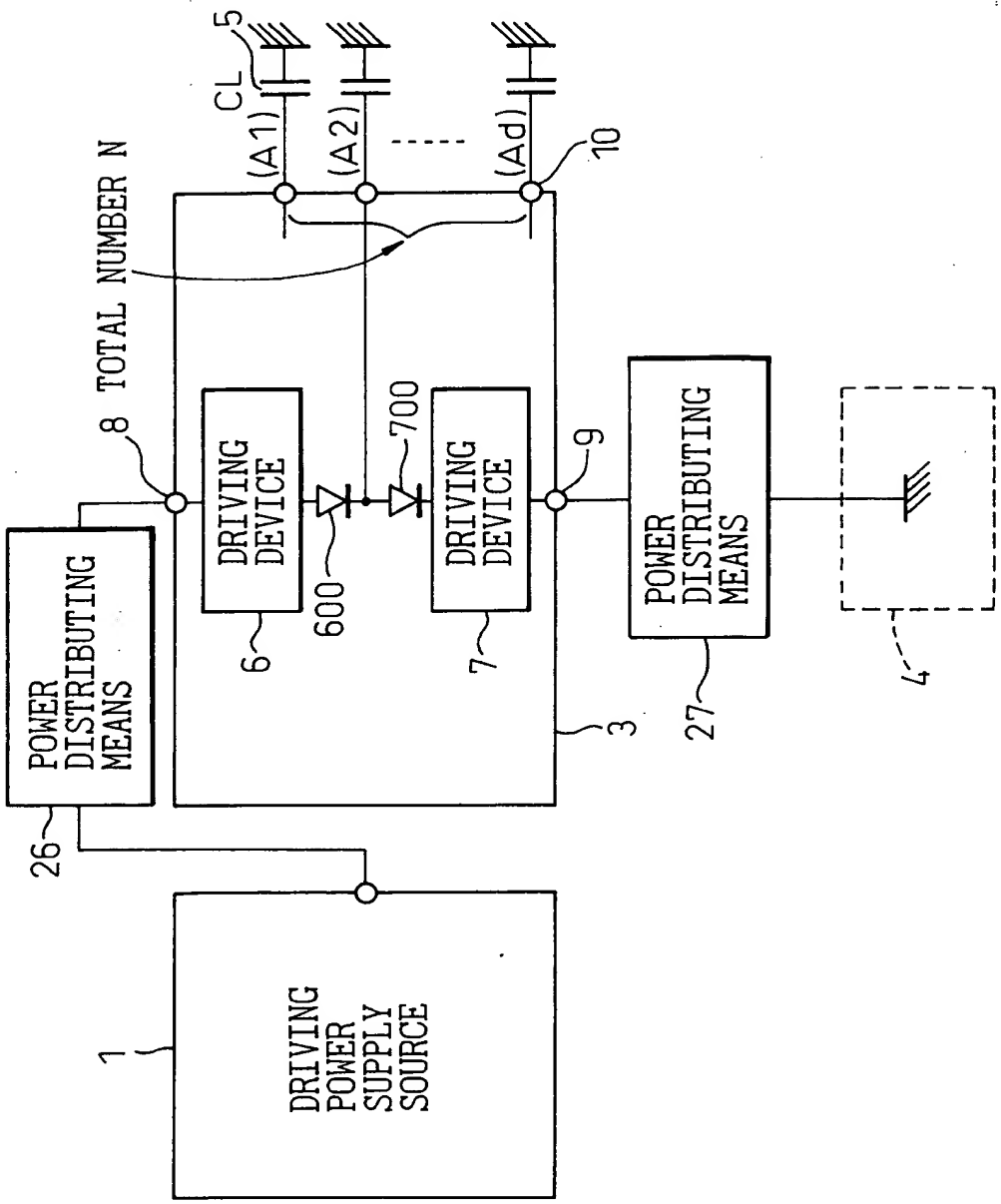

DRIVING POWER SUPPLY SOURCE
1
POWER DISTRIBUTING MEANS
26
8 TOTAL NUMBER N
DRIVING DEVICE
6
600
700
DRIVING DEVICE
7
9
3
POWER DISTRIBUTING MEANS
27
4
CL
5
(A1)
(A2)
(Ad)
10

Fig.14

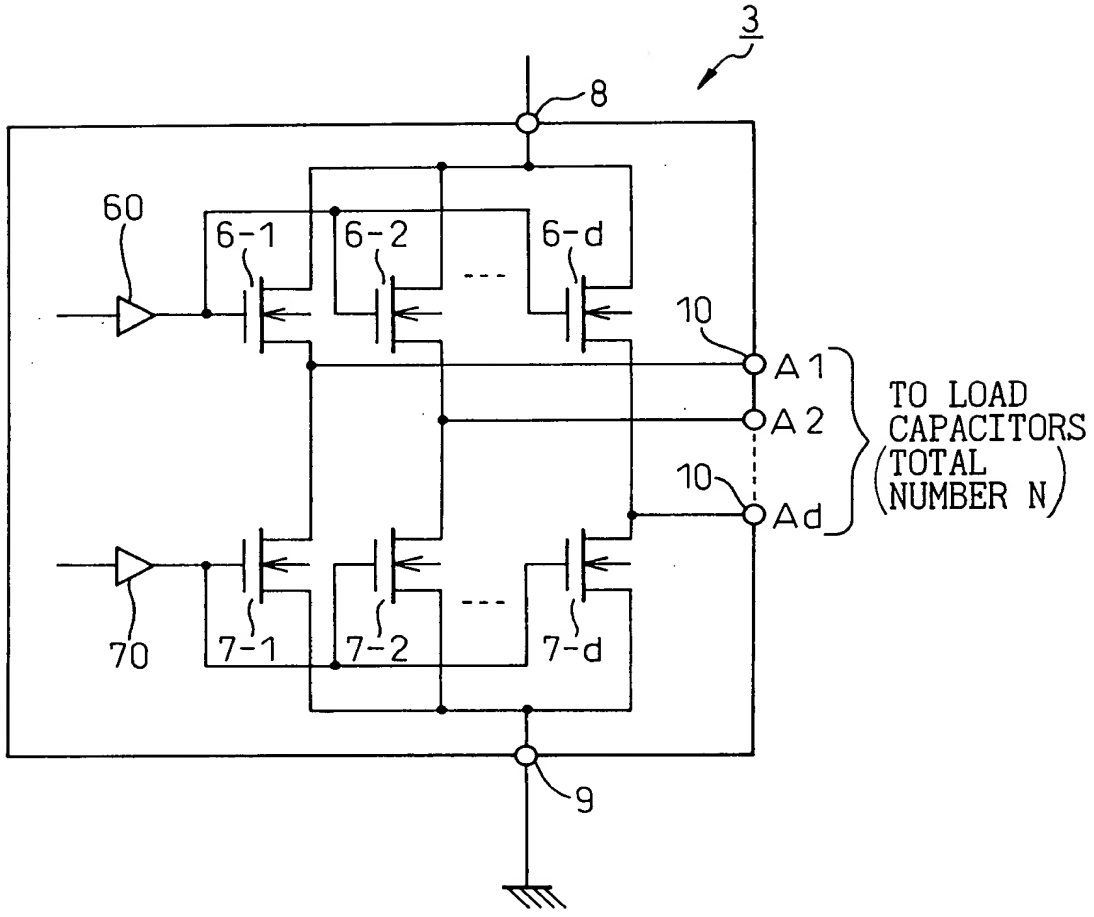

3
8
60
6-1
6-2
6-d
10
A1
A2
10
Ad
TO LOAD CAPACITORS (TOTAL NUMBER N)
70
7-1
7-2
7-d
9

Fig.15

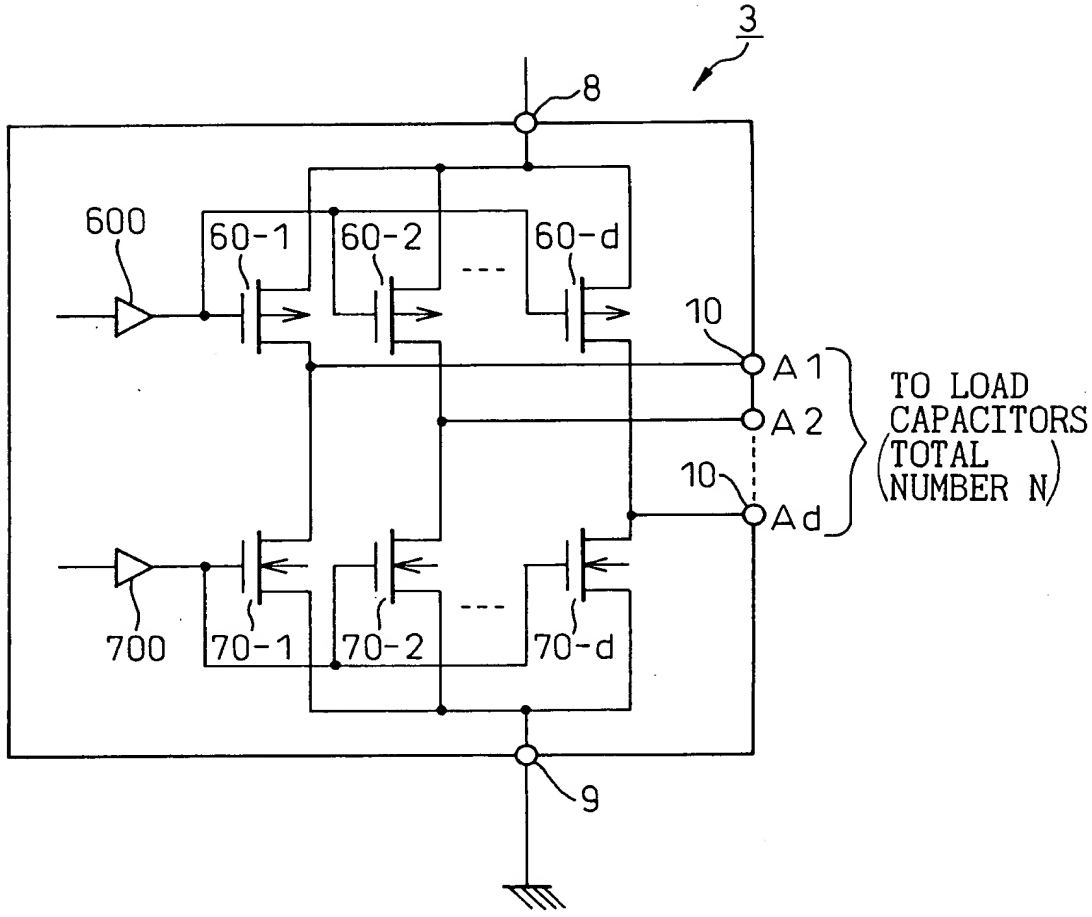

3
8
600
60-1
60-2
60-d
10
A1
A2
10
Ad
TO LOAD CAPACITORS (TOTAL NUMBER N)
700
70-1
70-2
70-d
9

Fig.16

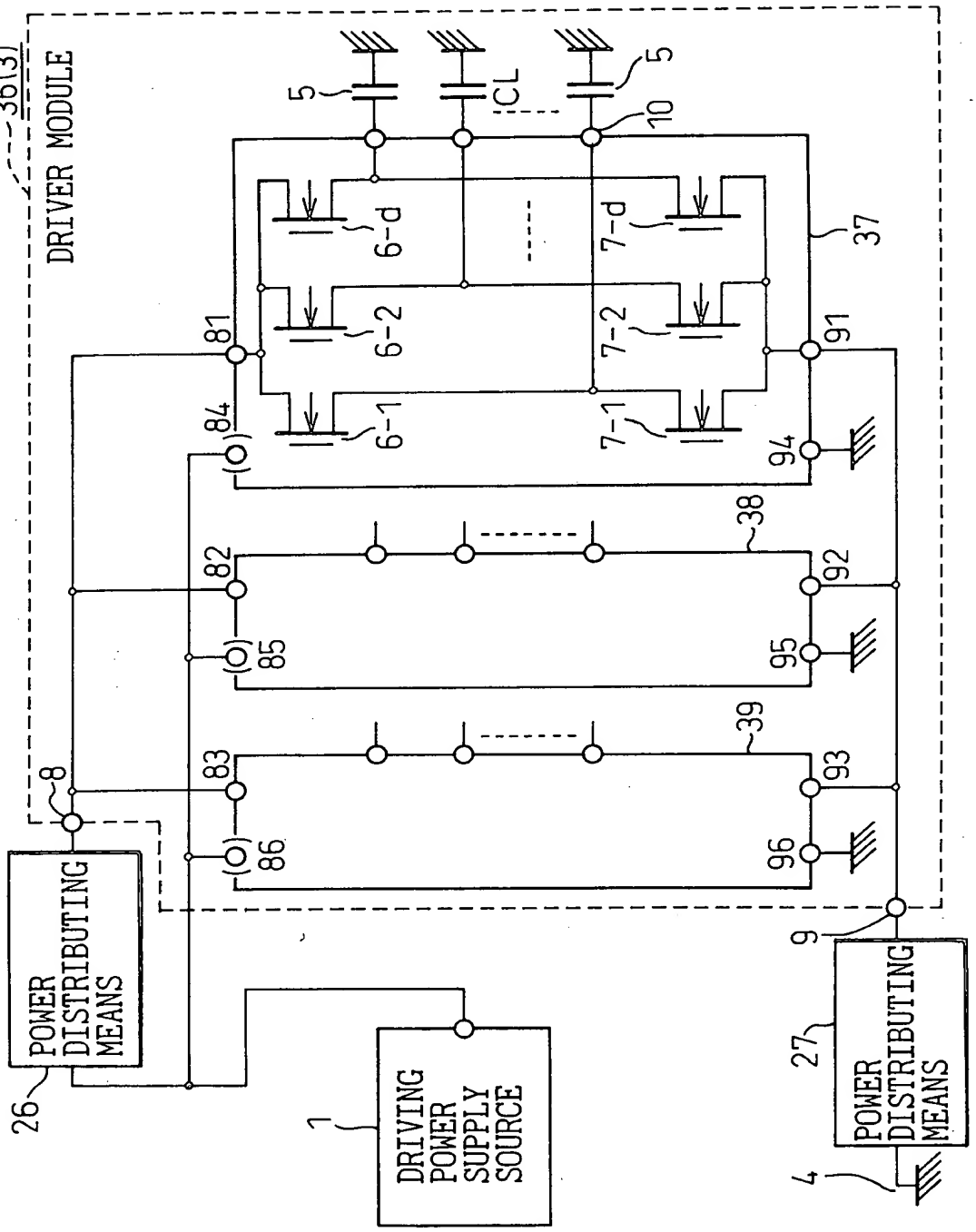

36(3)
DRIVER MODULE
5
CL
10
6-d
7-d
37
6-2
7-2
81
91
6-1
7-1
84
94
38
82
92
85
95
39
83
93
8
86
96
9
POWER DISTRIBUTING MEANS
26
DRIVING POWER SUPPLY SOURCE
1
27
POWER DISTRIBUTING MEANS
4

Fig.17

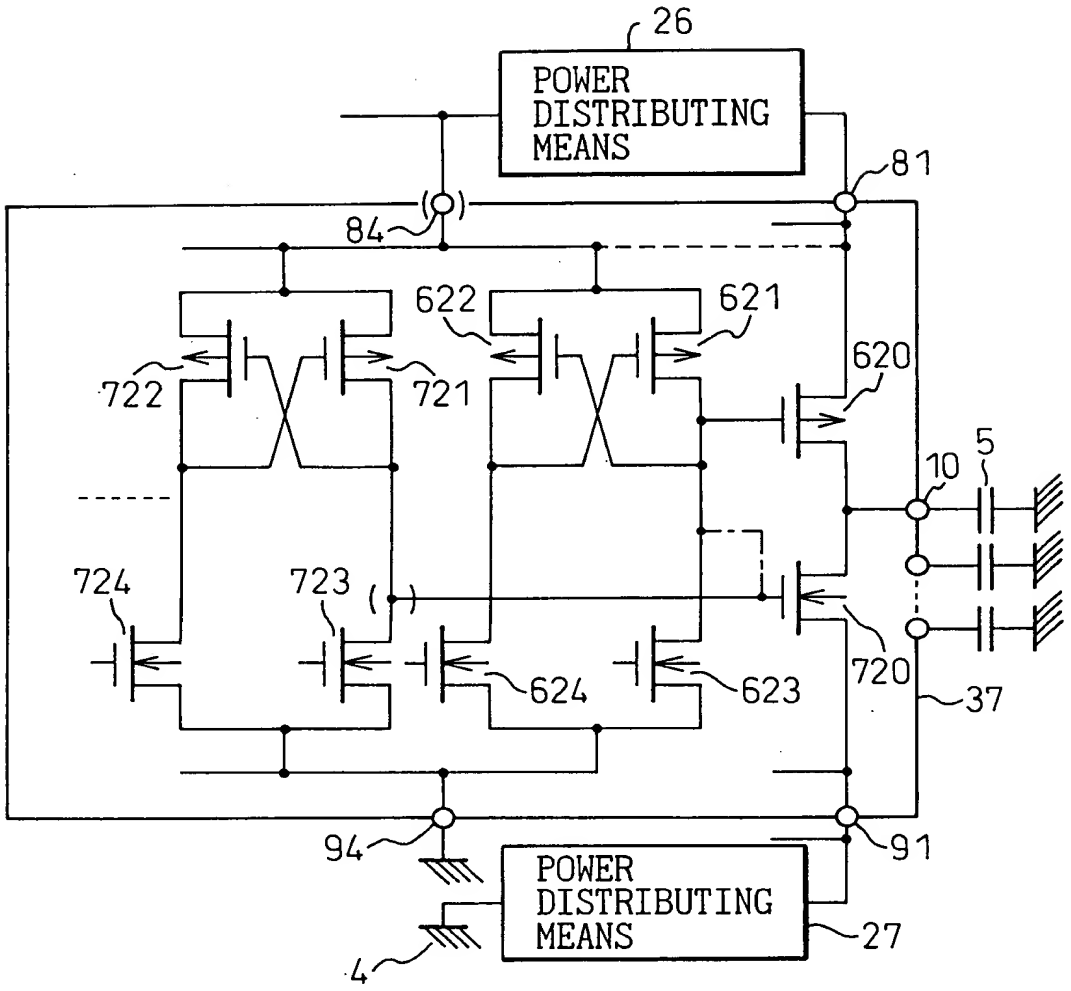

26
POWER DISTRIBUTING MEANS
81
84
622
621
722
721
620
10
5
724
723
624
623
720
37
94
91
POWER DISTRIBUTING MEANS
27
4

Fig.18

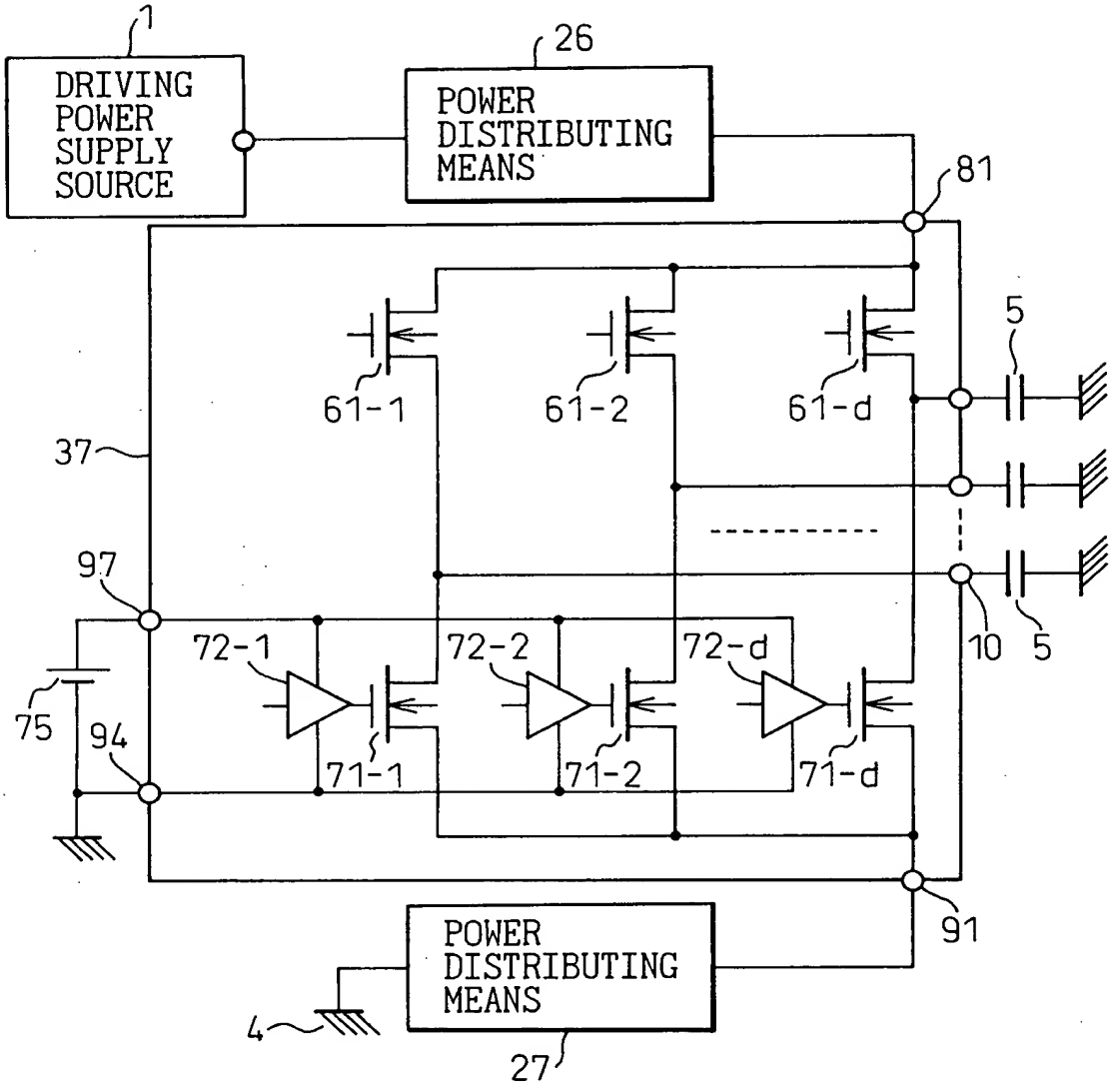

1
DRIVING POWER SUPPLY SOURCE
26
POWER DISTRIBUTING MEANS
81
5
61-1
61-2
61-d
37
97
72-1
72-2
72-d
10
5
75
94
71-1
71-2
71-d
91
POWER DISTRIBUTING MEANS
4
27

Fig.19

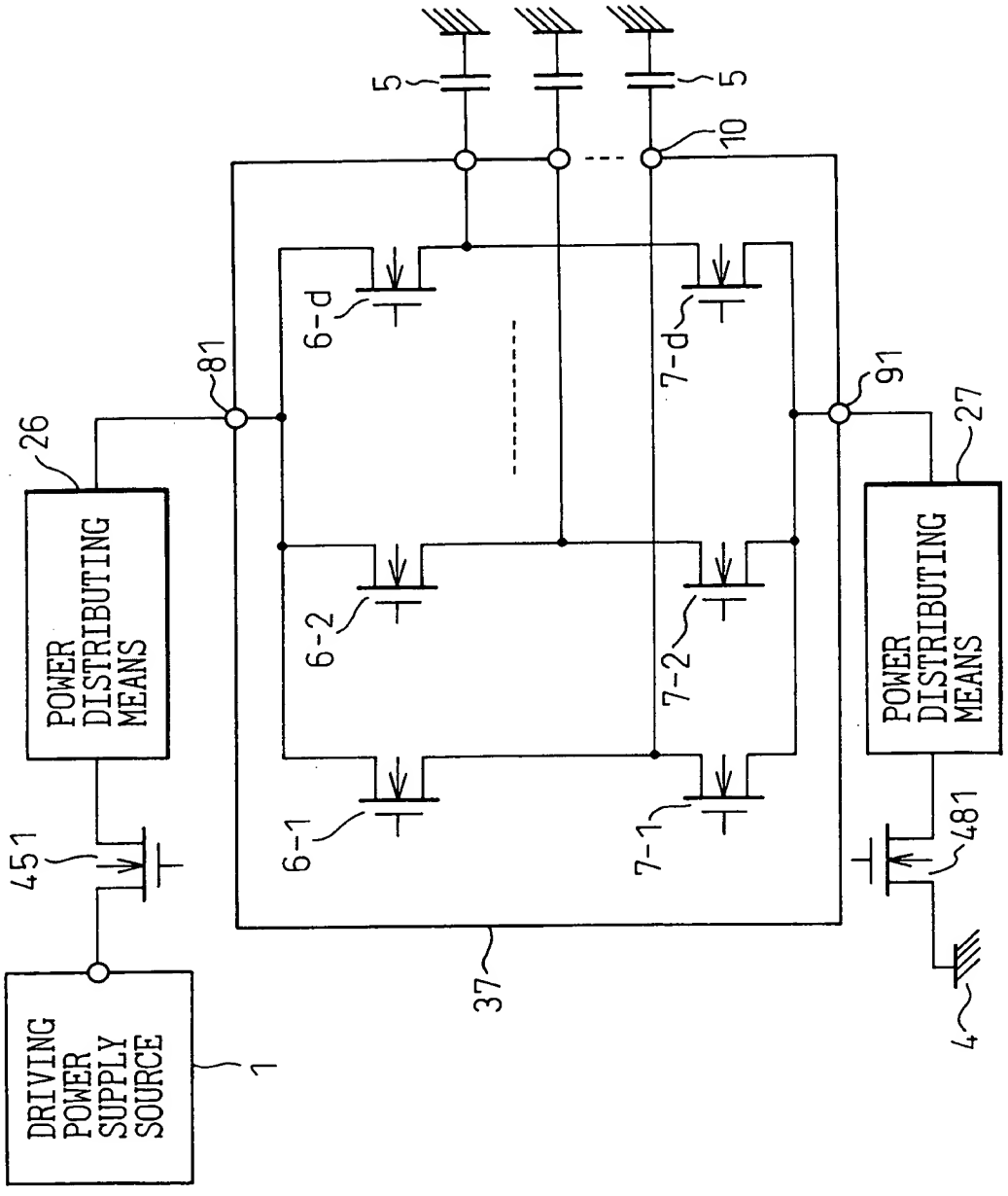

DRIVING POWER SUPPLY SOURCE
1
POWER DISTRIBUTING MEANS
26
POWER DISTRIBUTING MEANS
27
451
481
81
91
10
5
5
6-1
6-2
6-d
7-1
7-2
7-d
37
4

Fig.20

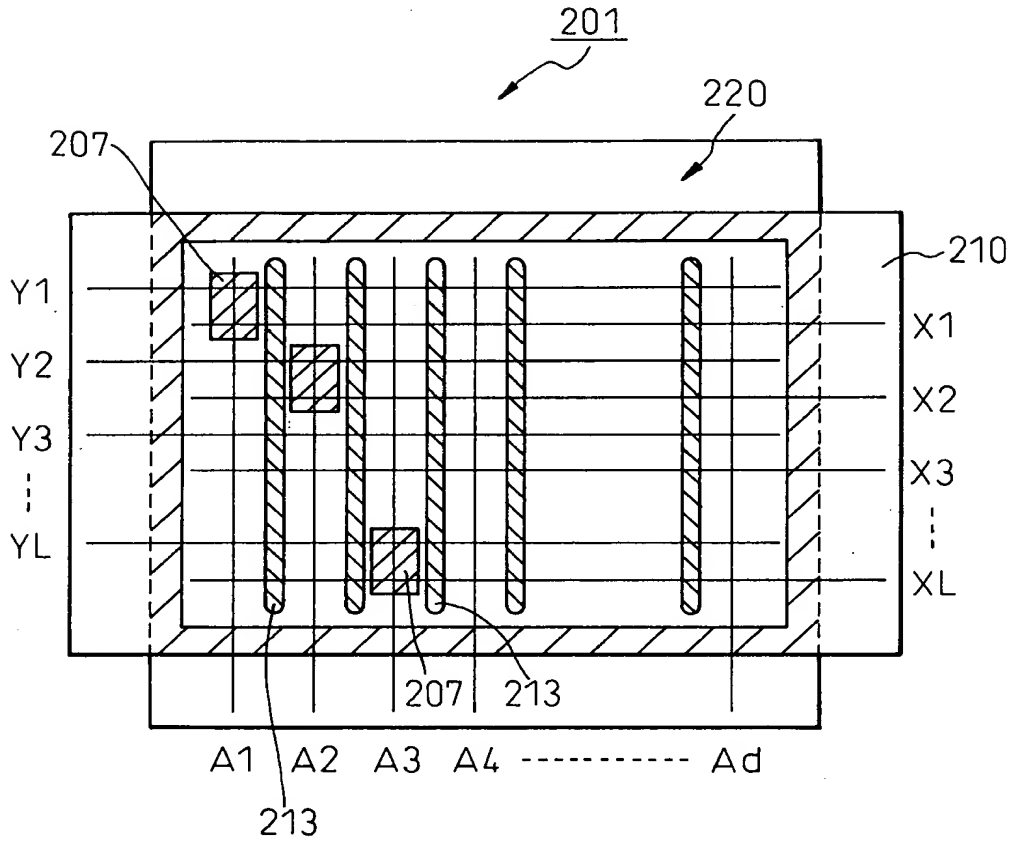


Fig.21

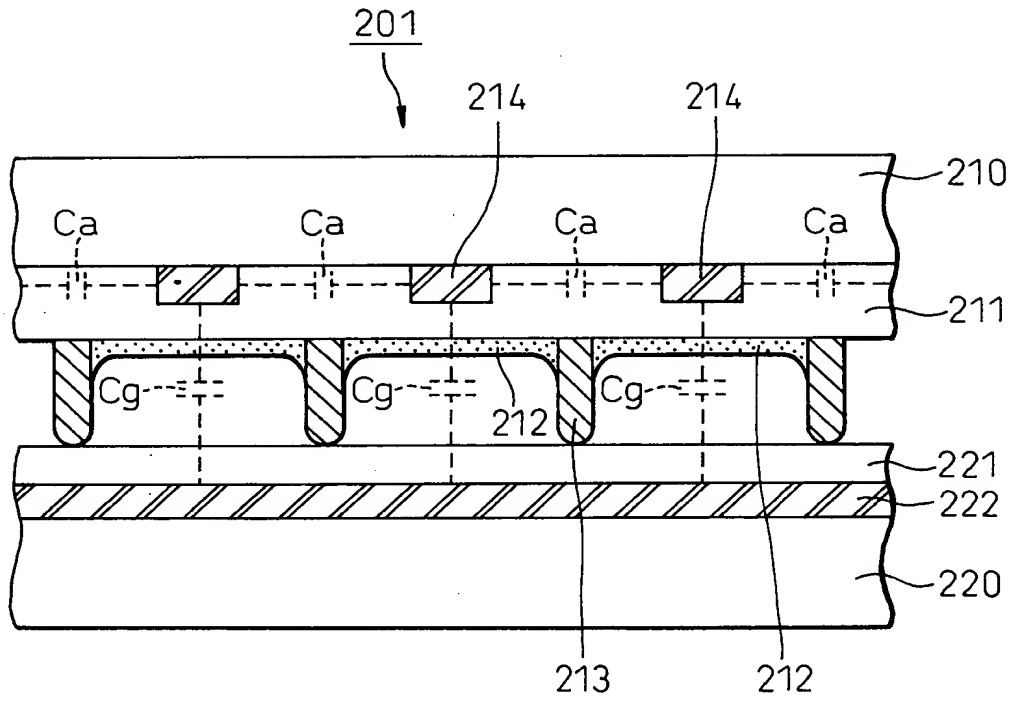


Fig.22

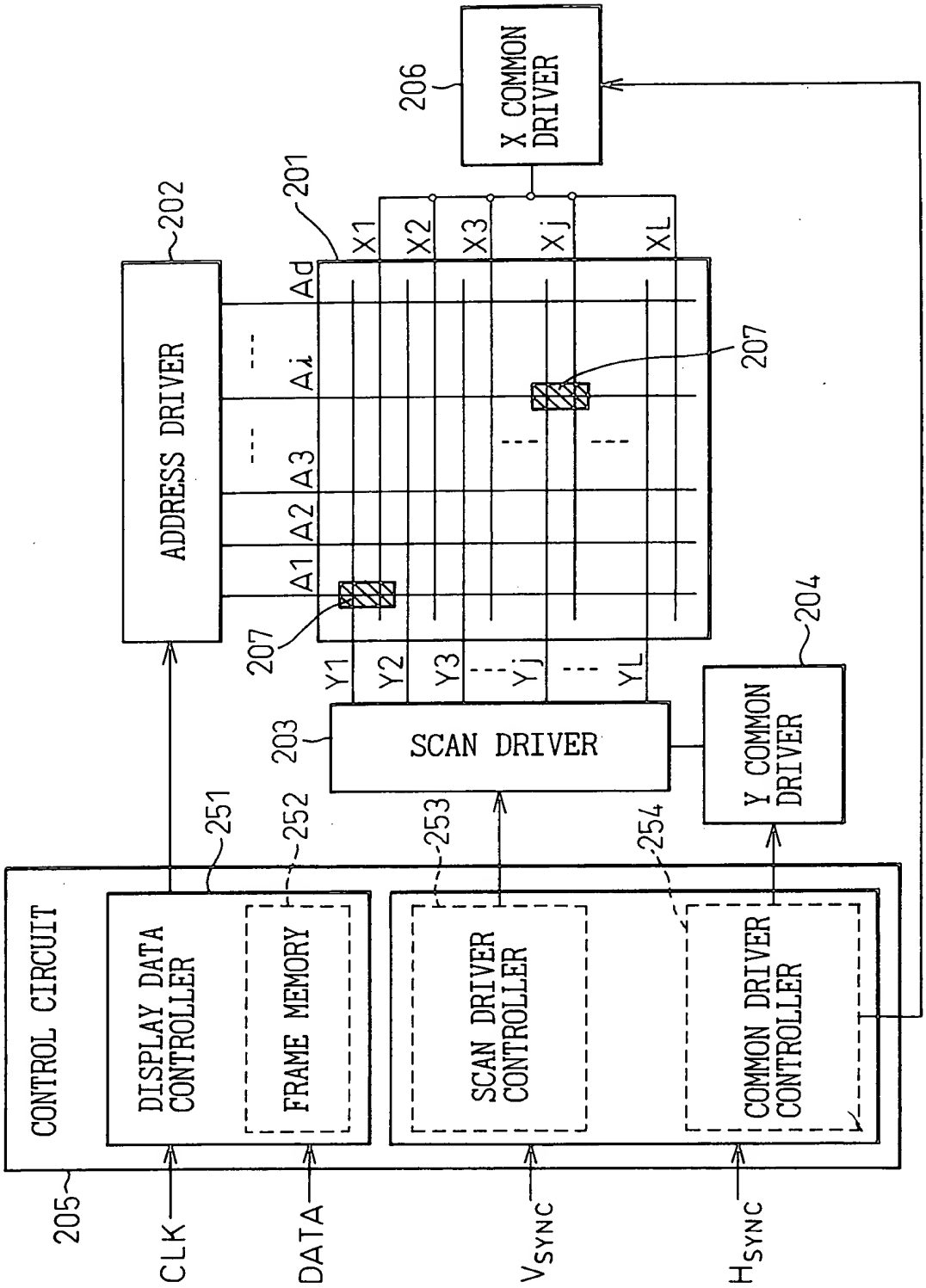

CONTROL CIRCUIT
DISPLAY DATA CONTROLLER
FRAME MEMORY
SCAN DRIVER CONTROLLER
COMMON DRIVER CONTROLLER
ADDRESS DRIVER
X COMMON DRIVER
Y COMMON DRIVER
SCAN DRIVER
205
CLK
DATA
VSYNC
HSYNC
251
252
253
254
202
206
204
203
201
207
A1
A2
A3
Ai
Ad
X1
X2
X3
Xj
XL
Y1
Y2
Y3
Yj
YL

Fig.23

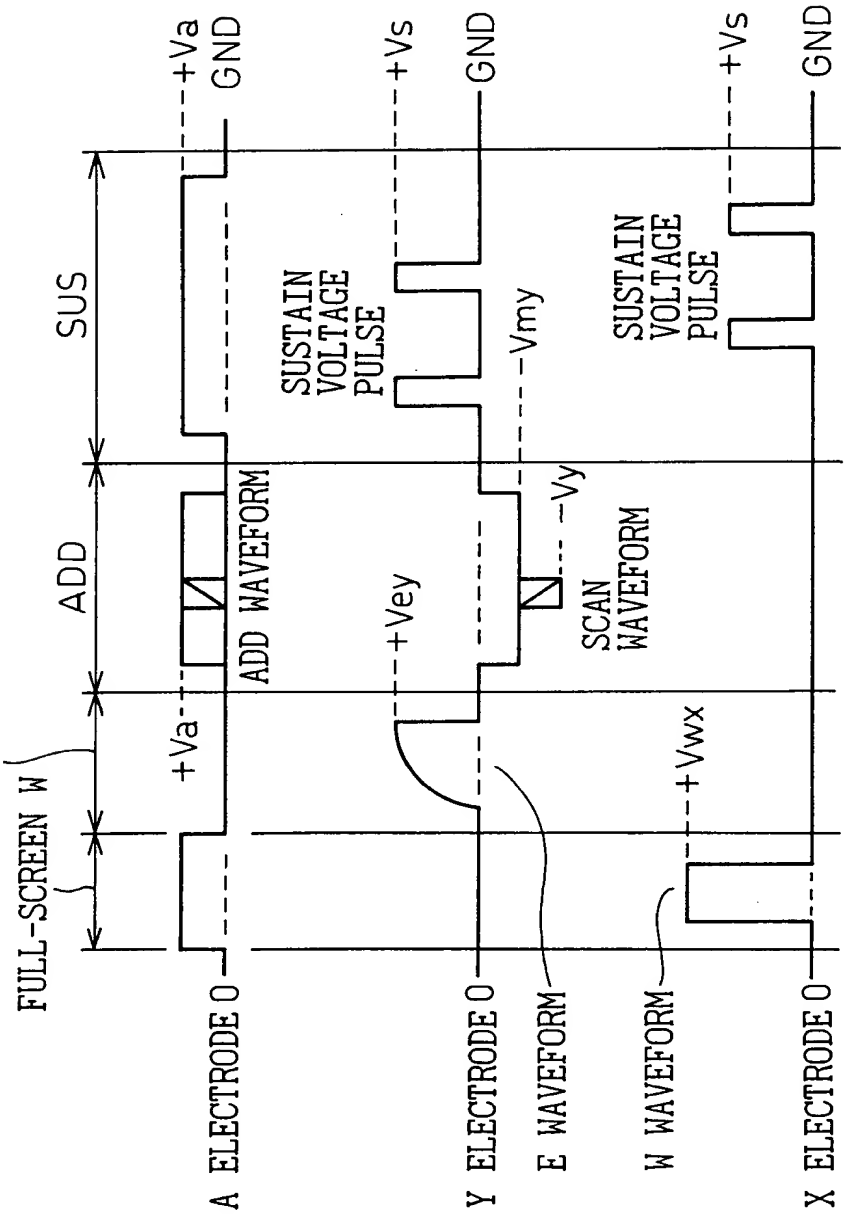

FULL-SCREEN E
FULL-SCREEN W
ADD
SUS
+Va
GND
+Va
ADD WAVEFORM
SUSTAIN VOLTAGE PULSE
+Vs
GND
+Vey
-Vy
-Vmy
SCAN WAVEFORM
SUSTAIN VOLTAGE PULSE
+Vs
GND
+Vwx
A ELECTRODE 0
Y ELECTRODE 0
E WAVEFORM
W WAVEFORM
X ELECTRODE 0

Fig.24

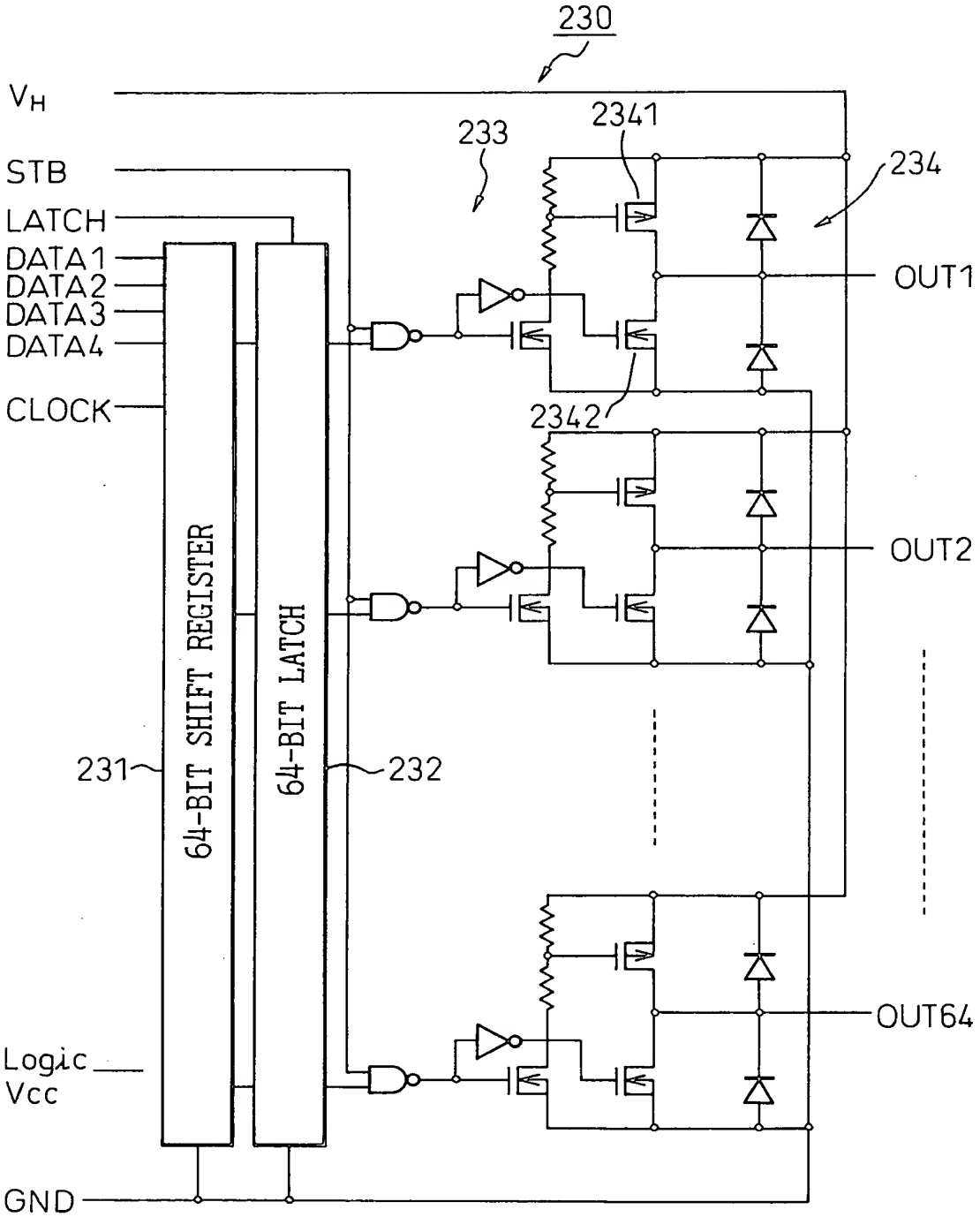

230
V_H
STB
LATCH
DATA1
DATA2
DATA3
DATA4
CLOCK
233
2341
234
OUT1
2342
OUT2
OUT64
64-BIT SHIFT REGISTER
64-BIT LATCH
231
232
Logic Vcc
GND

Fig.25

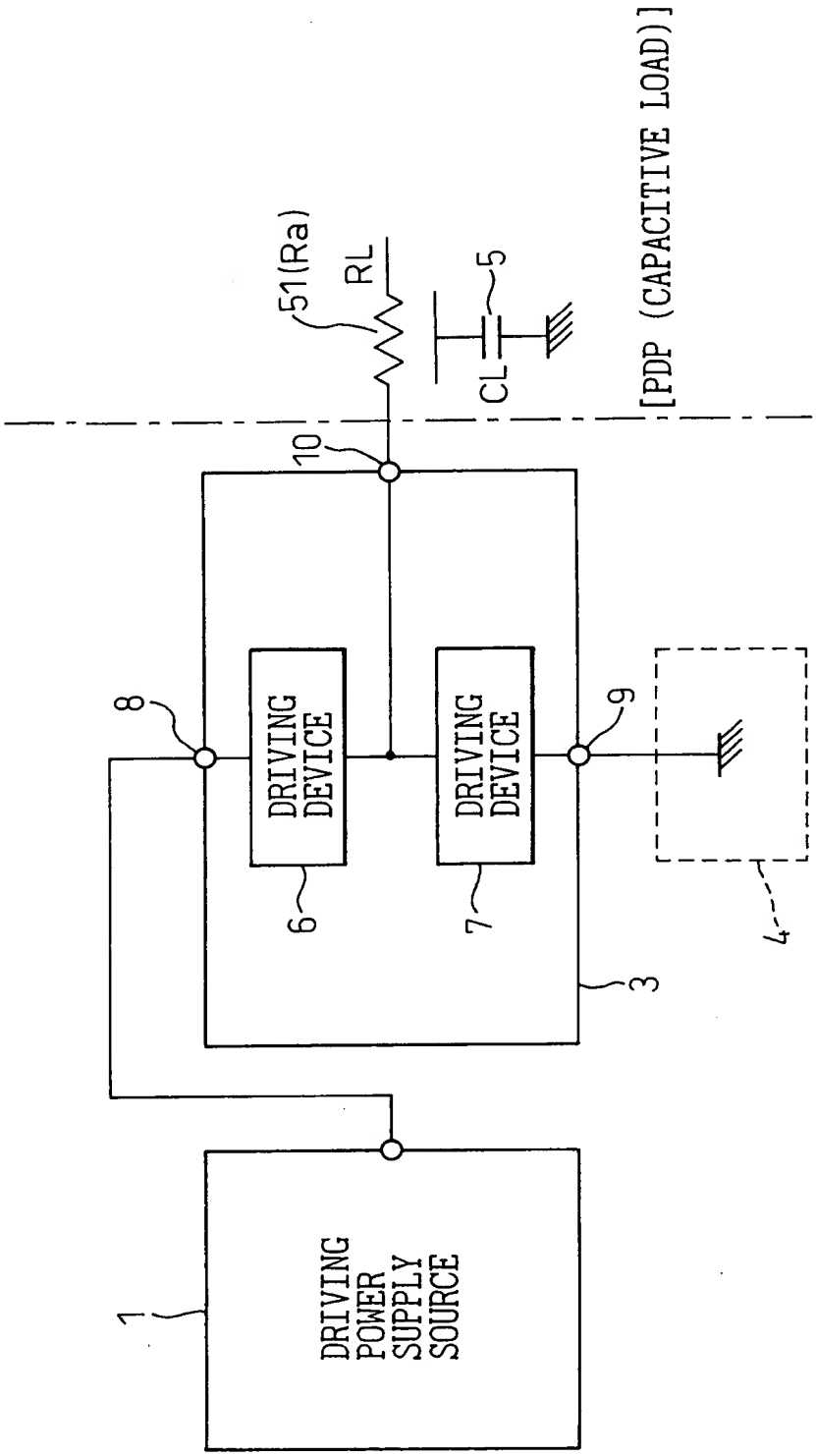

DRIVING POWER SUPPLY SOURCE
1
DRIVING DEVICE
6
DRIVING DEVICE
7
8
9
10
3
4
51(Ra)
RL
5
CL
[PDP (CAPACITIVE LOAD)]

Fig.26

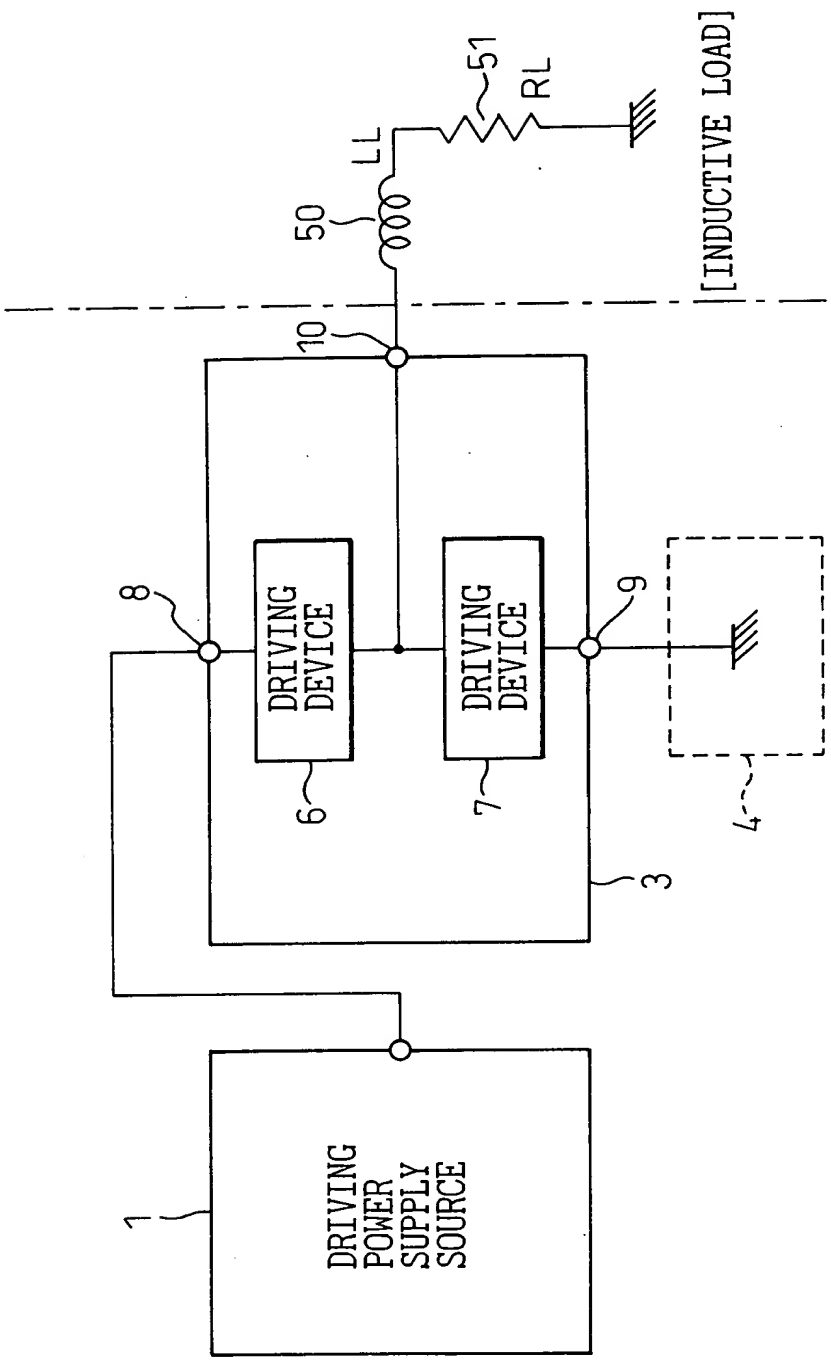

[INDUCTIVE LOAD]
50
LL
51
RL
10
8
DRIVING DEVICE
DRIVING DEVICE
9
6
7
4
3
1
DRIVING POWER SUPPLY SOURCE

Fig.27

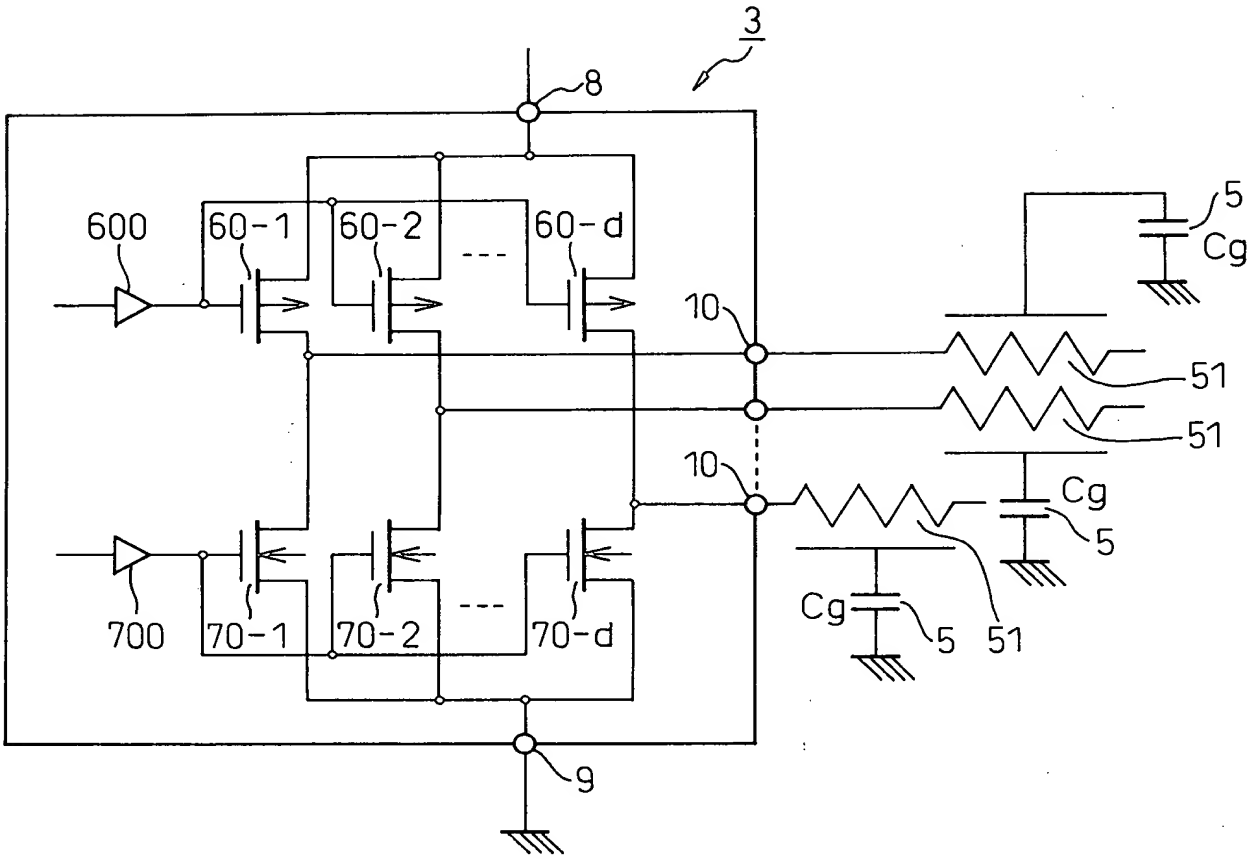


Fig.28A

SINGLE-MATERIAL ELECTRODE

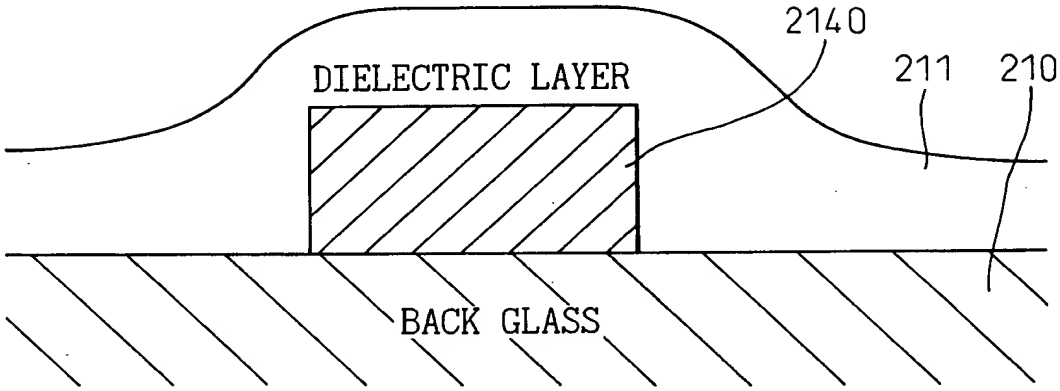


Fig.28B

COMPOSITE-MATERIAL ELECTRODE

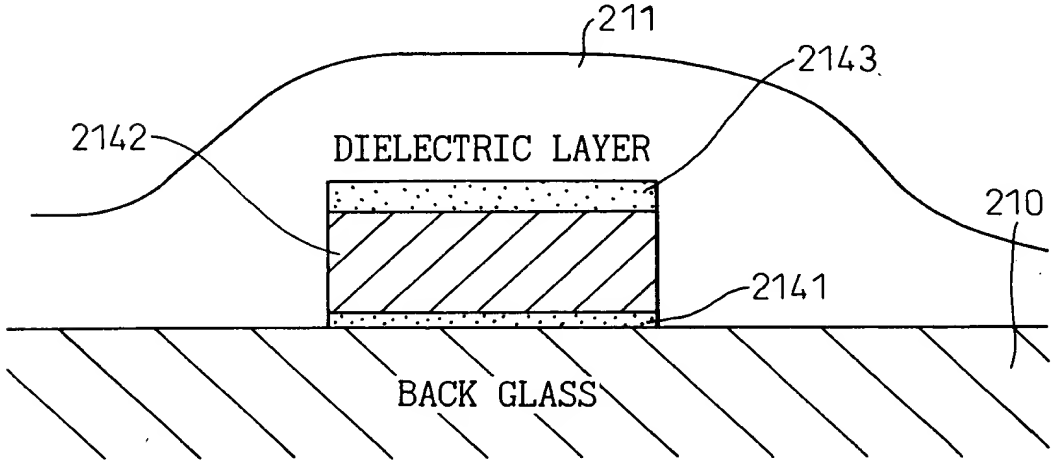
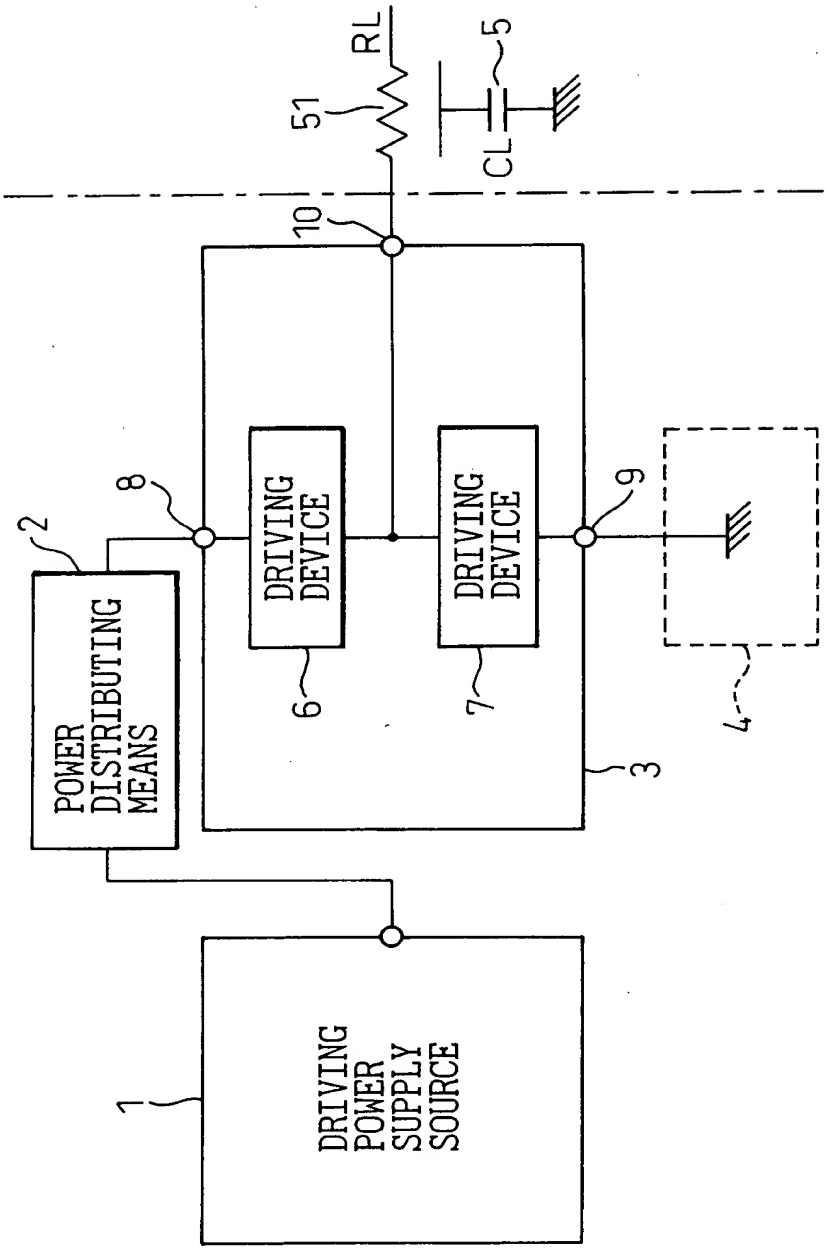


Fig.29


DRIVING POWER SUPPLY SOURCE
1
POWER DISTRIBUTING MEANS
2
DRIVING DEVICE
6
DRIVING DEVICE
7
8
9
10
3
4
51
RL
CL
5